

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

APPLICANT: Y. Kubota et al. CONF. NO.: 7275  
U.S. SERIAL NO.: 09/775,167 EXAMINER: S. Kumar  
FILED: February 1, 2001 GROUP: 2629  
FOR: SHIFT REGISTER CIRCUIT CAPABLE OF REDUCING  
CONSUMPTION OF POWER WITH REDUCED CAPACITIVE LOAD  
OF CLOCK SIGNAL LINE AND IMAGE DISPLAY DEVICE  
INCLUDING IT

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

**RESPONSE TO OFFICE ACTION**

Applicants are in receipt of the Office Action dated September 21, 2007 of the above-referenced application. Applicants respond to the Office Action as follows.

Claims 1-25 are pending in the application.

Claims 1-5, 14, and 25 were rejected under 35 USC 103(a) as being unpatentable over U.S. Patent 5,289,518 to Nakao in view of "Applicant's Admitted Prior Art (AAPA)." The remaining claims were rejected over prior art including the Nakao reference and AAPA. These rejections are respectfully traversed.

The proposed combination of Nakao in view of AAPA does not teach or suggest a shift register circuit in which an input control signal of a transfer gate of a corresponding register block is brought into an ON-state **only** in a specified period when an output of the corresponding flip-flop **changes**.

Please Enter March 30, 2008 /SKK/